AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A method for internal synchronization of a first and at least a second module which are within a single telecommunication device, and each ~~having~~ of which has a clock generator, the method comprising the steps of

- ~~transmitting~~ transmitting, by the first module, a first clock signal generated by its clock generator to the at least one second module,
- synchronizing the clock generator of the at least one second module with the first clock signal,
- ~~transmitting~~ transmitting, by the at least one second ~~module~~ module, a second clock ~~signal~~ signal, generated by ~~the~~ its clock ~~generator~~ generator, that is synchronized with the first clock signal to the first module,
- ~~determining~~ determining, by the first module, a ~~(first)~~ first time difference value between the first clock signal and the at least one second clock signal, which time difference value is essentially due to the transmission time of the first and the at least one second clock signal between the ~~first,~~ first and the at least one second module,
- ~~transmitting~~ transmitting, by the first module, an item of information about the ~~(first)~~ first time difference value to the at least one second ~~module~~ module, and

- adjusting the clock generator of the at least one second module on the basis of the information about the ~~(first)~~ first time difference value so that said first and second clock signals are synchronous,
- wherein the first time difference value is halved to adjust the clock generator of the at least one second module.

2. (canceled).

3. (currently amended): A method according to Claim 1, wherein the at least one second module determines a second time difference value from the first and the second clock ~~signal~~ signal, and wherein the at least one second module transmits an item of information about the second time difference value to the first module,.

4. (currently amended): A method according to Claim 1, wherein the first module cyclically transmits the first clock ~~signal~~ signal, generated by its clock ~~generator~~ generator, to the at least one second module at predetermined instants in ~~time, in particular cyclically.~~time.

5. (currently amended): A method according to Claim 1, wherein the first ~~module,~~ module retransmits the first clock ~~signal~~ signal, generated by its clock ~~generator~~ generator, to the at least one second module at predetermined time intervals, wherein the at least one second module determines a second time difference value from the first and the second clock ~~signal~~ signal, and

wherein the at least one second module transmits the respective second time difference value to the first module, and/or, if the respective second time difference value deviates from a predetermined value, ~~it~~ said second module adjusts its clock generator on the basis of the respective second time difference value .

6. (currently amended): A method according to Claim 1,

wherein the at least one second module retransmits the second clock ~~signal~~ signal, generated by its clock ~~generator~~ generator, to the first ~~module,~~ module at predetermined time intervals,

wherein the first ~~module,~~ module determines a first time difference value between the first clock signal and the respective second clock signal received,

wherein, if the respective first time difference deviates from a predetermined value, the first ~~module,~~ module transmits an item of ~~information~~ information, about the respective first time difference ~~value~~ value, to the at least one second ~~module~~ module, and

wherein the at least one second module adjusts its clock generator on the basis of the information about the respective first time difference value.

7. (currently amended): A ~~(first)~~ first module having a first clock generator for internal synchronization with at least one second module having a second clock generator, said first and second modules being within a single telecommunication device, said first module comprising

- transmitting means for transmitting a first clock signal generated by the first clock generator to the at least one second ~~module~~ module,
- receiving means for receiving at least one second clock signal generated by the respective second clock generator and synchronized with the first clock signal and transmitted by the at least one second module, and
- generating means for forming a ~~(first)~~ first time difference value between the first clock signal and the at least one second clock signal, which time difference value is essentially due to the transmission time of the first and of the at least one second clock signal between the ~~first,~~ first and the at least one second module,

~~and~~ wherein the transmitting means are designed for sending an item of information about the ~~(first)~~ first time difference value to the at least one second module.

8. (currently amended): A ~~(second)~~ second module having a clock generator for internal synchronization with at least one first module, said first and second modules being within a single telecommunication device, said second module comprising

- receiving means for receiving a first clock signal sent by the first module,
- synchronizing means for synchronizing its clock generator on the basis of the first clock ~~signal~~ signal, and
- transmitting means for sending a second clock signal synchronized with the first clock signal to the first module,

wherein the receiving means are designed for receiving an item of information sent by the first module about a ~~(first)~~ first time difference value formed from the first clock signal and the second clock signal, which time difference value is essentially due to the transmission time of the first and of the at least one second clock signal between the ~~first,~~ first and the at least one second module, and wherein the synchronizing means are designed for adjusting the clock generator on the basis of the information about the ~~(first)~~ first time difference value.

9. (currently amended): A master program module for a ~~(first)~~ first module having a first clock generator for internal synchronization with at least one second module having a second clock generator, wherein the first and second modules are within a single telecommunication device, and wherein the master program module contains a program code that can be run by a control means of the first module, the master program module further comprising

- transmitting means for sending a first clock signal generated by the first clock generator to the at least one second module,
- receiving means for receiving at least one second clock signal generated by the second clock generator that is synchronized with the first clock signal and sent by the at least one second module, and
- generating means for forming a ~~(first)~~ first time difference value between first clock signal and the at least one second clock signal, which time difference value is essentially due to the transmission time of the first and of the at least one second clock generator between the ~~first,~~ first and the at least one second module,

wherein the transmitting means are designed for sending an item of information about the (first) time difference value to the at least one second module.

10. (currently amended): A slave program module for a ~~(second)~~ second module having a clock generator for internal synchronization with at least one first module, wherein the first and second modules are within a single telecommunication device, and wherein the slave program module contains a program code that can be run by a control means of the second module, the slave program module further comprising

- receiving means for receiving a first clock signal sent by the first module,
- synchronizing means for synchronizing the clock generator on the basis of the first clock signal, and
- transmitting means for sending a second clock signal synchronized with the first clock signal to the first module,

wherein the receiving means are designed to receive an item of information transmitted by the first module about a ~~(first)~~ first time difference value formed from the first clock signal and the second clock signal, which time difference value is essentially due to the transmission time of the first and of the at least one second clock signal between the ~~first,~~ first and the at least one second module, and wherein the synchronizing means are designed to adjust the clock generator on the basis of the information about the ~~(first)~~ first time difference value.

11. (currently amended): A ~~device, in particular~~ telecommunication ~~device,~~ device containing therein at least one first and at least one second module, each having a clock generator, wherein the at least one first module comprises

- transmitting means for transmitting a first clock ~~signal~~ signal, generated by the first clock ~~generator~~ generator, to the at least one second module.
- receiving means for receiving at least one second clock signal generated by the respective second clock generator and synchronized with the first clock signal and transmitted by the at least one second module, and
- generating means for forming a ~~(first)~~ first time difference value between the first clock signal and the at least one second clock signal, which time difference value is essentially due to the transmission time of the first and of the at least one second clock signal between the first and the at least one second module,

wherein the transmitting means are designed for sending an item of information about the ~~(first)~~ first time difference value to the at least one second ~~module~~ module, and wherein the at least one second module comprises

- receiving means for receiving a first clock signal sent by the first module,
- synchronizing means for synchronizing its clock generator on the basis of the first clock signal, and
- transmitting means for sending a second clock ~~signal~~ signal, synchronized with the first clock ~~signal~~ signal, to the first module,

wherein the receiving means are designed for receiving an item of information sent by the first module about a ~~(first)~~ first time difference value formed from the first clock signal and the second clock signal, which time difference value is essentially due to the transmission time of the first and of the at least one second clock signal between the first and the at least one second module, ~~and~~ wherein the synchronizing means are designed for adjusting the clock generator of said second module on the basis of the information about the ~~(first)~~ first time difference value, and wherein the first time difference value is halved to adjust the clock generator of the at least one second module.

11. (canceled). Second occurrence of this claim 11 is to be canceled, beginning on page 22, line 6, with the words "A memory means". (This was previously canceled in the Preliminary Amendment filed March 19, 2004.)

12. (previously presented): A computer-readable diskette storing a master program module according to claim 9.

13. (previously presented): A computer readable diskette storing a slave program module according to claim 10.

14. (new) The method according to claim 1, further comprising the step of transmitting said first and second clock signals via bus lines interconnecting said first and said at least second module.

15. (new): The method according to claim 14, further comprising the steps of:

providing said first and second modules as respective spaced-apart printed circuit boards; and

providing said single telecommunication device as a telecommunication junction.

16. (new): The first module according to claim 7, wherein said first and second modules are respective spaced-apart printed circuit boards that are interconnected by bus lines via which said first and second clock signals are transmitted.

17. (new): The second module according to claim 8, wherein said first and second modules are respective spaced-apart printed circuit boards that are interconnected by bus lines via which said first and second clock signals are sent.

18. (new): The master program module according to claim 9, wherein said first and second modules are respective spaced-apart printed circuit boards that are interconnected by bus lines via which said first and second clock signals are sent.

19. (new): The slave program module according to claim 10, wherein said first and second modules are respective spaced-apart printed circuit boards that are interconnected by bus lines via which said first and second clock signals are sent.

20. (new) The device according to claim 11, wherein said first and second modules are respective spaced-apart printed circuit boards that are interconnected by bus lines via which said first and second clock signals are transmitted.